REMARKS

The Applicants thank the Examiner for the careful examination of this application and respectfully request the entry of the amendments indicated hereinabove.

Claims 1-18 are pending. Of the pending claim set, Claims 1-10 are rejected and Claims 11-18 are withdrawn from consideration. Claims 19-20 are new and Claims 1, 9, and 10 are amended hereinabove.

Independent Claim 1 positively recites forming a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions and forming an interfacial layer of nitrogen within the total exposed surface of the lightly-doped extension regions. These advantageously claimed features are not taught or suggested by the patents granted to Guo, Takenouchi et al., Liu, Hao et al., Moore, or Tseng et al.; either alone or in combination.

Guo does not teach the advantageously claimed invention because Guo does not teach forming a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions (column 3 lines 49-50; FIG. 2) and forming an interfacial layer of nitrogen within the total exposed surface of the lightly-doped extension regions (column 3 lines 49-55; FIGS. 2 and 4). Rather, Guo

teaches a nitrated gate dielectric (element 12 of FIG. 4, column 3 lines 13-22 and 31-34). (The Applicants note that the dielectric gate structure is a separately claimed element from the interfacial layer of nitrogen.) The Applicants respectfully traverse the statements in the Office Action (pages 3 and 4) that element 16 of Guo is both the layer of insulating material (page 3) and the sidewall layer (page 4). The Applicants submit that the sidewall layer and the interfacial layer of nitrogen are claimed as separate elements (that have separate and distinct labels); therefore, the "dielectric spacers 16" (column 3 line 25; FIG. 1) of Guo cannot teach both advantageously claimed elements. Moreover, the Applicants note that Guo does not teach forming an interfacial layer of nitrogen within the total exposed surface of the lightly-doped extension regions, as advantageously claimed (column 3 lines 49-55; FIGS. 2 and 4) or removing all of the capping layer after the annealing (column 4 lines 11-17).

Takenouchi et al. does not teach the advantageously claimed invention because Takenouchi et al. does not teach forming a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions (column 5 lines 3-7; FIG. 2E) and forming an interfacial layer of nitrogen within the total exposed surface of the lightly-doped extension regions (column 4 lines 8-49). The Applicants respectfully traverse the statements in the Office Action (pages 4-5) that Takenouchi et al. teaches the formation of an insulation layer after forming the LDD. The Applicants submit that element 16 of Takenouchi et al. is the dielectric gate

structure that is a separately claimed element from the claimed layer of insulating material (plus element 36 is a sidewall layer that is also a separately claimed element from the claimed layer of insulating material). (The Applicants also note that the sidewalls of Guo and Takenouchi et al. are not "in contact with a total exposed surface of the lightly-doped extension regions" as advantageously claimed.) In addition, the Applicants respectfully traverse the statements in the Office Action (page 5) that one of ordinary skill in the art would combine the teachings of Guo and Takenouchi et al. The Applicants submit that one of ordinary skill in the art would not combine a method of forming a transistor having the lightly doped region 18 and the heavily doped region 20 of Guo (column 3 lines 49-51) with the dual diffusion lightly doped layers 32, 38 and the heavily doped layer 22 Takenouchi et al. (column 4 lines 48-49 and 53-55) because the transistor of Guo would have vastly different operating characteristics (and correspondingly have different electronic system applications) than the transistor of Takenouchi et al. having a "step like" doping profile formed with a two-step (and thereby a more expensive) fabrication process (column 5 lines 62-68).

Liu does not teach the advantageously claimed invention because Liu does not teach forming a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions (column 4 lines 12-15; FIG. 5) and forming an interfacial layer of nitrogen within the total exposed surface of the lightly-doped extension regions (column 3 lines 39-45). The Applicants respectfully

traverse the statements in the Office Action (page 6) that FIGS. 3-4 of Liu teaches the claimed formation of a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions. The Applicants submit that FIG. 4 of Liu teaches the deposition of a layer of nitride (column 3 lines 48-53) that is immediately etched to form the sidewalls that are a separately claimed element than the layer of insulating material (column 4 lines 1-5; FIG. 5). Furthermore, the Applicants respectfully traverse the assertion in the Office Action (page 7) that a combination of Guo, Takenouchi et al., and Liu teaches the claimed invention. The Applicants submit that no combination of Guo, Takenouchi et al., and Liu teaches the separate elements of a dielectric gate structure, at least one sidewall layer, a layer of silicon oxide in contact with a total exposed surface of the lightly-doped extension regions, and an interfacial layer of nitrogen within the total exposed surface of the lightly-doped extension regions.

Hao et al. does not teach the advantageously claimed invention because Hao et al. does not teach forming a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions (column 3 line 30 through column 4 line 3; FIGS. 2A-9) and forming an interfacial layer of nitrogen within the total exposed surface of the lightly-doped extension regions (column 3 line 30 through column 4 line 3; FIGS. 2A-9). Moreover, Hao et al. does not teach the formation of lightly doped extension regions (column 3 line 30 through column 4 line 3; FIGS. 2A-9). The Applicants respectfully traverse the statements in the Office

Action (page 7) that Hao et al teaches the claimed invention in column 3 lines 17-26. The Applicants submit that in column 3 lines 17-26 Hao et al. generally discusses the implantation of nitrogen generally into the source/drain regions, but Hao et al. doesn't teach the advantageously claimed method of forming an interfacial layer of nitrogen within the total exposed surface of the lightly-doped extension regions. Moreover, the Applicants respectfully traverse the statement in the Office Action (page 7) that Hao et al teaches implanting "an additional layer of nitrogen into the...LDD regions" in column 3 lines 17-26. The Applicants submit that the LDD regions are not discussed in column 3 lines 17-26 (or anywhere else) in Hao et al.

Moore does not teach the advantageously claimed invention because Moore does not teach forming a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions (paragraphs 0020, 0023, 0031; FIGS. 3-4) and forming an interfacial layer of nitrogen within the total exposed surface of the lightly-doped extension regions (paragraphs 0020, 0023, 0031; FIGS. 3-4). Rather, Moore teaches the use of a sidewall layer that contains silicon nitride (paragraphs 0020, 0023, 0031; FIGS. 3-4). The Applicants respectfully traverse the assertion in the Office Action (page 9) that one of ordinary skill in the art would combine the teachings of Guo, Takenouchi et al., and Moore. The Applicants submit that one of ordinary skill in the art would not combine a method of forming a transistor having extensions (18) and source/drain (20) (Guo FIG. 2) with a method

of forming a transistor having two extensions (32, 38) and source/drain (22) (Takenouchi et al. FIG. 2D) or with a method of forming a transistor having only a source/drain (19) (Moore FIG. 4).

Tseng et al. does not teach the advantageously claimed invention because Tseng et al. does not teach forming a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions (column 4 lines 1-44, FIG. 9) and forming an interfacial layer of nitrogen within the total exposed surface of the lightly-doped extension regions (column 4 lines 1-44, FIG. 9). Moreover, Tseng et al. does not teach the formation of lightly doped extension regions (column 4 lines 6-7; FIG. 8). The Applicants respectfully traverse the assertion in the Office Action (page 11) that combining the multilayered gate dielectric of Tseng et al. with the single layer gate dielectric Guo will teach the advantageously claimed layer of insulating material. The Applicants submit that the dielectric gate structure and the layer of insulating material are separately claimed elements. Therefore, the multilayered gate dielectric of Tseng et al. does not teach or suggest any aspect of the layer of insulating material. In addition, the Applicants respectfully traverse the assertion in the Office Action (page 12) that one of ordinary skill in the art would combine the teachings of Tseng et al. with Guo. The Applicants submit that one of ordinary skill in the art would not combine a method of making a transistor having a multilayered gate structure (Tseng et al.) with a method of making a transistor having a gate structure comprised of only a layer of silicon dioxide (Guo) because

the transistors would have different operating parameters (and therefore different device applications) and different cost basis (because a multilayered gate dielectric is more costly to make due to the extra manufacturing steps and the corresponding reduction in manufacturing yield).

Therefore, the combination of Guo, Takenouchi et al., Liu, Hao et al., Moore, and Tseng et al. also does not teach forming a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions and forming an interfacial layer of nitrogen within the total exposed surface of the lightly-doped extension regions, as advantageously claimed.

Regarding Claim 5, the Applicants traverse the assertion (on page 8 of the Office Action) that Claim 2 of Guo teaches the advantageously claimed insulating layer of Claim 5. The Applicants submit that Claim 2 of Guo is directed to the gate dielectric (column 5 line 1); however, the gate dielectric cannot be the advantageously claimed insulating layer of Claim 5 because the advantageously claimed insulating layer is a separately claimed element from the dielectric gate structure and the insulating layer is formed over the total surface of the LDD regions (see Applicants' Claim 1). The gate dielectric layer of Guo (element 12 of FIGS. 2 and 4) is not formed over the LDD (as positively recited in the Applicants' Claim 1).

Regarding Claim 6, the Applicants respectfully traverse the assertion (on page 8 of the Office Action) that Claim 4 of Guo teaches the advantageously claimed methods of thermal annealing, plasma treatment, or N implantation. The Applicants submit that Claim 4 of Guo lists the composition of gases for the nitridizing step but does not specify the claimed method for incorporating nitrogen (such as the claimed N_2 plasma treatment).

Regarding Claim 8, the Applicants respectfully traverse the assertion (on pages 8-9 of the Office Action) that Claim 22 of Guo teaches the advantageously claimed time range of less than 10 seconds. The Applicants submit that Claim 22 of Guo does not specify the advantageously claimed time range. In addition, the Applicants respectfully traverse the assertion (on page 9 of the Office Action) that Claim 22 of Guo teaches the advantageously claimed temperature range of 1000-1100 degrees centigrade. The Applicants submit that Claim 22 of Guo specifies the temperature range of 800-1000 degrees centigrade, but Guo does not specify the advantageously claimed temperature range. The Applicants note that one of ordinary skill in the art knows that the temperature range of 800-1000 degrees centigrade taught by Guo does not prompt the lateral diffusion of the extension and source/drain dopants towards the gate stack; therefore the method of Guo teaches away from the advantageously claimed step of forming an interfacial layer of nitrogen due to the added cost of the step.

Due to the foregoing reasons, the Applicants respectfully traverse the Examiner's rejection of Claim 1 and respectfully assert that Claim 1 is patentable over the patents granted to Guo, Takenouchi et al., Liu, Hao et al., Moore, and Tseng et al.; either alone or in combination. Furthermore, Claims 2-9 and 19 are allowable for depending on allowable independent Claim 1 and, in combination, including limitations not taught or described in the references of record.

Independent Claim 10 positively recites forming a layer of silicon oxide in contact with a total exposed surface of the lightly-doped extension regions and forming an interfacial layer of nitrogen within the total exposed surface of the lightly-doped extension regions. These advantageously claimed features are not taught or suggested by the patents granted to Guo, Takenouchi et al., Liu, Hao et al., or Tseng et al.; either alone or in combination.

Guo does not teach the advantageously claimed invention because Guo does not teach forming a layer of silicon oxide in contact with a total exposed surface of the lightly-doped extension regions (column 3 lines 49-50; FIG. 2) and forming an interfacial layer of nitrogen within the total exposed surface of the lightly-doped extension regions (column 3 lines 49-55; FIGS. 2 and 4). Rather, Guo teaches a nitrated gate dielectric (element 12 of FIG. 4, column 3 lines 13-22 and 31-34). The Applicants note that the Office Action (pages 10-11) does not state the element of FIG. 4 that teaches the claimed layer of silicon oxide, the element of FIG.

4 that teaches the claimed interfacial layer of nitrogen, or the element of FIG. 4 that teaches the claimed capping layer of contiguous silicon nitride. Furthermore, the Applicants note that Guo does not teach forming an interfacial layer of nitrogen within the total exposed surface of the lightly-doped extension regions, as advantageously claimed (column 3 lines 49-55; FIGS. 2 and 4). Moreover, the Applicants respectfully traverse the assertion (on page 11 of the Office Action) that Claim 22 of Guo teaches the advantageously claimed step of removing the nitride cap after the annealing. The Applicants submit that Claim 22 of Guo specifies the temperature range of 800-1000 degrees centigrade, but Claim 22 does not specify removing the nitride cap after the annealing.

Takenouchi et al. does not teach the advantageously claimed invention because Takenouchi et al. does not teach forming a layer of silicon oxide in contact with a total exposed surface of the lightly-doped extension regions (column 5 lines 3-7; FIG. 2E) and forming an interfacial layer of nitrogen within the total exposed surface of the lightly-doped extension regions (column 4 lines 8-49). The Applicants respectfully traverse the statements in the Office Action (page 12) that Takenouchi et al. teaches the formation of an insulation layer after forming the LDD. The Applicants submit that element 16 of Takenouchi et al. is the dielectric gate structure that is a separately claimed element from the claimed layer of insulating material (plus element 36 is a sidewall layer that is also a separately claimed element from the claimed layer of insulating material). (The

Applicants also note that the sidewalls of Guo and Takenouchi et al. are not "in contact with a total exposed surface of the lightly-doped extension regions" as advantageously claimed.) The Applicants also respectfully traverse the assertion in the Office Action (page 12) that element 16 of Takenouchi et al. is the claimed layer of silicon oxide. The Applicants submit that element 16 of Takenouchi et al. is the dielectric gate structure (column 3 lines 21-22 and 67-68; FIGS. 1-2) that is a separately claimed element than the claimed layer of silicon oxide. In addition, the Applicants respectfully traverse the statements in the Office Action (page 12) that it would be obvious to combine the teachings of Guo and Takenouchi et al. The Applicants submit that one of ordinary skill in the art would not combine a method of forming a transistor having the lightly doped region 18 and the heavily doped region 20 of Guo (column 3 lines 49-51) with the dual diffusion lightly doped layers 32, 38 and the heavily doped layer 22 Takenouchi et al. (column 4 lines 48-49 and 53-55) because the transistor of Guo would have vastly different operating characteristics (and correspondingly different electronic system applications) than the transistor of Takenouchi et al. having a "step like" doping profile formed with a two-step (and thereby a more expensive) fabrication process (column 5 lines 62-68).

Liu does not teach the advantageously claimed invention because Liu does not teach forming a layer of silicon oxide in contact with a total exposed surface of the lightly-doped extension regions (column 4 lines 12-15; FIG. 5) and

forming an interfacial layer of nitrogen within the total exposed surface of the lightly-doped extension regions (column 3 lines 39-45). The Applicants respectfully traverse the statements in the Office Action (page 12) that FIGS. 3-4 of Liu teaches the claimed formation of a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions. The Applicants submit that FIG. 4 of Liu teaches the deposition of a layer of nitride (column 3 lines 48-53) that is immediately etched to form the sidewalls that are a separately claimed element than the layer of insulating material (column 4 lines 1-5; FIG. 5). Furthermore, the Applicants respectfully traverse the assertion in the Office Action (page 13) that a combination of Guo, Takenouchi et al., and Liu teaches the claimed invention. The Applicants submit that no combination of Guo, Takenouchi et al., and Liu teaches the separate elements of a dielectric gate structure, at least one sidewall layer, a layer of silicon oxide in contact with a total exposed surface of the lightly-doped extension regions, and an interfacial layer of nitrogen within the total exposed surface of the lightly-doped extension regions.

Hao et al. does not teach the advantageously claimed invention because Hao et al. does not teach forming a layer of silicon oxide in contact with a total exposed surface of the lightly-doped extension regions (column 3 line 30 through column 4 line 3; FIGS. 2A-9) and forming an interfacial layer of nitrogen within the total exposed surface of the lightly-doped extension regions (column 3 line 30

through column 4 line 3; FIGS. 2A-9). Moreover, Hao et al. does not teach the formation of lightly doped extension regions at all (column 3 line 30 through column 4 line 3; FIGS. 2A-9). The Applicants respectfully traverse the statements in the Office Action (page 14) that Hao et al teaches the claimed invention in column 3 lines 17-26. The Applicants submit that in column 3 lines 17-26 Hao et al. generally discusses implantation into the source/drain regions, but Hao et al. doesn't teach the advantageously claimed method of forming an interfacial layer of nitrogen within the total exposed surface of the lightly-doped extension regions. Moreover, the Applicants respectfully traverse the statement in the Office Action (page 14) that Hao et al teaches implanting "an additional layer of nitrogen into the...LDD regions" in column 3 lines 17-26. The Applicants submit that the LDD regions are not discussed in column 3 lines 17-26 (or anywhere else) in Hao et al.

Tseng et al. does not teach the advantageously claimed invention because Tseng et al. does not teach forming a layer of silicon oxide in contact with a total exposed surface of the lightly-doped extension regions (column 4 lines 1-44, FIG. 9) and forming an interfacial layer of nitrogen within the total exposed surface of the lightly-doped extension regions (column 4 lines 1-44, FIG. 9). Moreover, Tseng et al. does not teach the formation of lightly doped extension regions anywhere (column 4 lines 6-7; FIG. 8). The Applicants respectfully traverse the assertion in the Office Action (page 11) that combining the multilayered gate dielectric of Tseng

et al. with single layer gate dielectric of Guo will teach the advantageously claimed layer of silicon oxide. The Applicants submit that the dielectric gate structure and the layer of silicon oxide are separately claimed elements. Therefore, the multilayered gate dielectric of Tseng et al. does not teach or suggest any aspect of the layer of silicon oxide. In addition, the Applicants respectfully traverse the assertion in the Office Action (page 12) that one of ordinary skill in the art would combine the teachings of Tseng et al. with Guo. The Applicants submit that one of ordinary skill in the art would not combine a method of making a transistor having a multilayered gate structure (Tseng et al.) with a method of making a transistor having a gate structure comprised of only a layer of silicon dioxide (Guo) because the transistors would have different operating parameters (and therefore different device applications) and different cost basis (because a multilayered gate dielectric is more costly to make due to the extra manufacturing steps and the corresponding reduction in manufacturing yield).

Therefore, the combination of Guo, Takenouchi et al., Liu, Hao et al., and Tseng et al. also does not teach forming a layer of silicon oxide in contact with a total exposed surface of the lightly-doped extension regions and forming an interfacial layer of nitrogen within the total exposed surface of the lightly-doped extension regions, as advantageously claimed.

The Applicants respectfully traverse the assertion (on page 8-9 of the Office Action) that Claim 22 of Guo teaches the advantageously claimed time range of less than 10 seconds. The Applicants submit that Claim 22 of Guo does not specify the advantageously claimed time range. In addition, the Applicants respectfully traverse the assertion (on pages 9 and 17 of the Office Action) that Claim 22 of Guo teaches the advantageously claimed temperature range of 1000-1100 degrees centigrade. The Applicants submit that Claim 22 of Guo specifies the temperature range of 800-1000 degrees centigrade, but Guo does not specify the advantageously claimed temperature range.

Due to the foregoing reasons, the Applicants respectfully traverse the Examiner's rejection of Claim 10 and respectfully assert that Claim 10 is patentable over the patents granted to Guo, Takenouchi et al., Liu, Hao et al., and Tseng et al.; either alone or in combination. Furthermore, Claim 20 is allowable for depending on allowable independent Claim 10 and, in combination, including limitations not taught or described in the references of record.

For the reasons stated above, this application is believed to be in condition for allowance. Reexamination and reconsideration is requested.

Respectfully submitted,

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